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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/867,137	05/29/2001	Joseph J. Ervin	P6451	7466
45774	7590	02/10/2005	EXAMINER	
KUDIRKA & JOBSE, LLP ONE STATE STREET, SUITE 800 BOSTON, MA 02109			KING, JUSTIN	
			ART UNIT	PAPER NUMBER
			2111	

DATE MAILED: 02/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<p align="center">Office Action Summary</p>	Application No. 09/867,137	Applicant(s) ERVIN, JOSEPH J.	
	Examiner Justin I. King	Art Unit 2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 December 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9, 11-19 and 21-30 is/are pending in the application.
- 4a) Of the above claim(s) 21-30 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 and 11-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 5/29/01 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-9 and 11-19 in the reply filed on 12/29/04 is acknowledged.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the bridge address and tunnel command in claims 1 and 11 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified

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and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-7 and 11-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the Schutte (U.S. Patent No. 6,092,138) and "PCI-to-PCI Bridge Architecture Specification" by PCISIG.

Referring to claim 1: Schutte discloses a bridged segmented I2C bus system connecting master devices and slave devices (figure 1), which is the claimed limitation (a). Schutte's each bus segment connects both master and slaves devices, which is part of the claimed limitation (c). Schutte discloses connecting the I2C with a bridge, and the message forwarding is a part of the bridge functions, which is a part of limitation (d). Although the message forwarding is a part of the bridge function, Schutte does not explicitly disclose selectively forwarding. Schutte does not

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explicitly disclose the message's address format/tunnel command and the bridge ID. Although Shutte discloses a bridge between buses, Shutte is silent about how bridge should transmit message between buses. A person with ordinary skill in the computer art in seeking for bridge functions of Shutte will look at other system utilizing the bridge between the bus segments to determine how to operate a bridge.

A related bus architecture PCI utilizes the bridge between bus segments. The PCI specification teaches a message format with the address. The PCI spec discloses a Type 0 and Type 1 transaction types (page 19) with the different values in the bits [1::0]. The PCI spec discloses selectively forwarding the transaction and command from one bus segment to another depending on the values in bits [1::0]. Since the Type 1 is designated to the bridge and to reach devices on another side of the bridge, the bits [1::0] in PCI spec is equivalent to an address designating the message to the bridge. The PCI spec discloses that the message format includes bus number bits [23::16], device number bits [15::11], function number bits [10::8], and register number [7::2]. The bits [15::2] in the PCI spec is equivalent to the claimed tunnel command, which includes data and device address. Since PCI's device address [15::11] is lower than the bus number [23::16], the PCI spec supports the same device address on different bus segments. The PCI spec further discloses the Type 1 to Type 0 conversion (page 21), which is the bridge receiving the tunnel command, extracting the slave device address, and forwarding the data to the extracted slave device address on the second bus segment.

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt the teachings of the PCI message format onto Shutte

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because the PCI spec teaches one to format the message to support activities and to transmit messages between bus segments.

Referring to claim 2: The PCI Spec discloses a mapping (page 25).

Referring to claim 3: The PCI Spec discloses a based register and a limit register (page 25, 1Ch), which are the claimed pair of range registers.

Referring to claim 4: The PCI Spec discloses a tree hierarchy (page 12, figure 1-1).

Referring to claim 5: The PCI Spec discloses entering information into the address bitmap (page 25, Section 3.2).

Referring to claim 6: The PCI Spec discloses a bus master at the root level (page 12, figure 1-1, the CPU).

Referring to claim 7: Schutte discloses a bi-directional bridge (figure 1, structure 14).

Referring to claim 11: Schutte discloses a bridged segmented I2C bus system connecting master devices and slave devices (figure 1), which is the claimed limitation (a). Schutte's each bus segment connects both master and slaves devices, which is part of the claimed limitation (c). Schutte discloses connecting the I2C with a bridge, and the message forwarding is a part of the bridge functions, which is a part of limitation (d). Although the message forwarding is a part of the bridge function, Schutte does not explicitly disclose selectively forwarding. Schutte does not explicitly disclose the message's address format/tunnel command and the bridge ID. Although Schutte discloses a bridge between buses, Schutte is silent about how bridge should transmit message between buses. A person with ordinary skill in the computer art in seeking for bridge functions of Schutte will look at other system utilizing the bridge between the bus segments to determine how to operate a bridge.

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A related bus architecture PCI utilizes the bridge between bus segments. The PCI specification teaches a message format with the address. The PCI spec discloses a Type 0 and Type 1 transaction types (page 19) with the different values in the bits [1::0]. The PCI spec discloses selectively forwarding the transaction and command from one bus segment to another depending on the values in bits [1::0]. Since the Type 1 is designated to the bridge and to reach devices on another side of the bridge, the bits [1::0] in PCI spec is equivalent to an address designating the message to the bridge. The PCI spec discloses that the message format includes bus number bits [23::16], device number bits [15::11], function number bits [10::8], and register number [7::2]. The bits [15::2] in the PCI spec is equivalent to the claimed tunnel command, which includes data and device address. Since PCI's device address [15::11] is lower than the bus number [23::16], the PCI spec supports the same device address on different bus segments. The PCI spec further discloses the Type 1 to Type 0 conversion (page 21), which is the bridge receiving the tunnel command, extracting the slave device address, and forwarding the data to the extracted slave device address on the second bus segment.

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt the teachings of the PCI message format onto Shutte because the PCI spec teaches one to format the message to support activities and to transmit messages between bus segments.

Referring to claim 12: The PCI Spec discloses a mapping (page 25).

Referring to claim 13: The PCI Spec discloses a based register and a limit register (page 25, 1Ch), which are the claimed pair of range registers.

Referring to claim 14: The PCI Spec discloses a tree hierarchy (page 12, figure 1-1).

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Referring to claim 15: The PCI Spec discloses entering information into the address bitmap (page 25, Section 3.2).

Referring to claim 16: The PCI Spec discloses a bus master at the root level (page 12, figure 1-1, the CPU).

Referring to claim 17: Schutte discloses a bi-directional bridge (figure 1, structure 14).

6. Claims 8-9 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schutte, the PCI Spec, and Jennings (U.S. Patent No. 5,632,021).

Referring to claims 8 and 18: Schutte and the PCI Spec's disclosures are stated above, none of them explicitly discloses two unidirectional bridges. Jennings discloses two unidirectional bridges (figure 3, structures 331 and 332) to connect two bus segments (figure 3, structures buses 0 and 1). Jennings teaches one to prevent the livelock caused by one bus master monopolizing the bus and excluding the bus master from another bus. Jennings separates the upstream and downstream bridge transactions in order to prevent the livelock. Hence, it would have been obvious to one having ordinary skill in the computer art to adapt Jennings' bi-bridge architecture onto Schutte and the PCI application because Jennings teaches one to prevent the livelock by separating the upstream and downstream transactions.

Referring to claims 9 and 19: The PCI specification discloses that each device including the bridges has a configuration register (Section 3.2). The configuration register has the vendor ID and device ID, which are the bridge ID.

Response to Arguments

7. In response to Applicant's argument that the claimed tunnel command contains both data and a slave device address that appears as data in the command (Remark, page 8, last paragraph, last 6 lines): The PCI spec discloses a Type 0 and Type 1 transaction types (page 19) with the different values in the bits [1::0]. The PCI spec discloses selectively forwarding the transaction and command from one bus segment to another depending on the transaction type. The PCI spec discloses that the message format includes bus number bits [23::16], device number bits [15::11], function number bits [10::8], and register number [7::2]. The bits [15::2] in the PCI spec is equivalent to the claimed tunnel command, which includes data and device address.
8. In response to Applicant's argument regarding the Perlman (Remark, page 9, last paragraph, page 10, paragraphs 1-4): The argument is moot in view of the new ground(s) of rejection.
9. In response to Applicant's argument that Schutte does not address the address exhaustion (Remark, page 9, 1st paragraph, last 3 lines): The rejection above applies the teaching of the PCI message format to specify devices with same device address.

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Conclusion

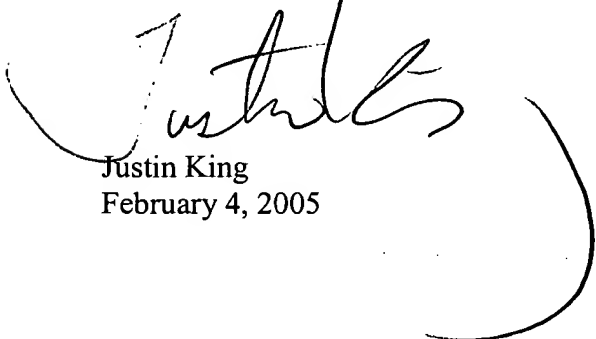
10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 5,675,794 to Meredith: Meredith discloses that each bridge has a bridge ID (figure 3, structure 320) in a multiple bridge structure. Meredith teaches that the unique bridge ID is needed to determine which bridge of the multiple bridges is responsible for the bus activities (column 8, lines 57-66, column 10, lines 6-13).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin I. King whose telephone number is 571-272-3628. The examiner can normally be reached on Monday through Friday, 9:00 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Justin King
February 4, 2005



MARK W. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100